In the Drawings:

Enclosed are a set of drawings labeled Replacement Sheets. These drawings have been corrected per the Examiner's comments, but contain no new matter.

REMARKS

The application was filed with 24 claims, claims 1-24. By this paper, claims 10 and 24 have been canceled. Hence, claims 1-9, and 11-23 are represented for further examination. Claims 1, 12, 18, and 29 have been amended.

The drawings stand objected to for various reasons. With respect to FIG. 2, the drawings are objected to because connections between comparator 52 and both the receive and transmit registers as described in the specification, are not shown. Further with respect to FIG. 2, FIG. 2 includes a reference character 40 which is not referenced in the specification. Also, the array 104 in FIG. 5 contains an incomplete descriptor. Still further, claim 5 is objected to for containing an incomplete line of connection between control logic 116 and registers 110 and 112. Lastly, the drawings are objected to as failing to include reference character 110 in FIG. 5.

With this paper, substitute drawings for sheets 1-5 are provided. Sheets 1, 3, and 4 are provided for the sole reason that an inadvertent error in the title of the application is included at the top of each drawing sheet. For these reasons and additional reasons, new drawing sheets 2 and 5 are also provided. New drawing sheet 2 includes the connections between the comparator 52 and the receive register 54 and programmable transmit register 56. Also, reference character 18 has been corrected and communication line 44 has now been indicated as being a parallel data communication line. With respect to FIG. 5, it is also being resubmitted because the descriptor for the register array 104 has been modified as required, reference character 110 has been included, and the connection between logic control 116, register 110, and register 112 has been deemed corrected.

In view of the foregoing, it is respectfully requested that the substitute sheets of drawings be accepted. It is respectfully submitted that no new matter has been added to any of the amendments made to the drawings.

With respect to the claims, claim 1 is rejected under 35 U.S.C. § 112, 2nd paragraph, as being indefinite. The Examiner considers to be unclear whether the transmit register of line 3 transmits data to the serializer, deserializer, or both serializer and deserializer. Claim 1 is also considered to be indefinite because of the

use of the term "processed data" in line 4 and in lines 5 and 7. It is alleged that the process data of lines 5 and 7 cannot be the same process data recited in line 4.

In response to the 35 U.S.C. § 112 rejection of claim 1, it will be noted that claim 1 has been extensively amended so as to be clearly definite. As will be noted, the term "serializer/deserializer" has been replaced by the term "data processing". Hence, in keeping with the disclosure in the application, the serializer/deserializer has been treated as a single circuit and hence the use of the term data processing circuit is considered to be appropriate. Further, in claim 1, the data processing circuit is defined as being arranged to serialize and deserialize received parallel data into processed parallel data. As a result, the term data processing circuit is clearly meant to define a circuit which both serializes and then deserializes inputted parallel data. As a result, the data transmitted by the transmit register is now defined as transmitted "parallel data" and the data resulting from the serializing and deserializing by the data processing circuit is defined as "processed parallel data". It is respectfully submitted that these amendments clearly clarify any previous indefiniteness.

Claims 10, 12, and 18 have been similarly rejected under 35 U.S.C. § 112, 2nd paragraph. In response thereto, it will be noted that these claims have also been amended in an essentially identical manner as claim 1. As a result, it is respectfully submitted that the 35 U.S.C. § 112 rejection of claims 1, 10, 12, and 18 has been obviated.

Lastly, claim 21 is considered to provide sufficient antecedent basis for the term "the transmitted data". Accordingly, claim 21 has been amended by defining the first method step as transmitting programmably varying parallel data to a data processing circuit which, it is respectfully submitted, provides proper antecedent basis for the "transmitted data" recitation which follows. Accordingly, it is respectfully submitted that claim 21 has been amended to provide sufficient antecedent basis for the term "the transmitted data".

With respect to the prior art, claims 1, 2, 5-7, 10-12, 14, 15, 18, 19, 21, and 22 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Takinosawa, U.S. Patent No. 6,977,960. It is respectfully submitted that amendments made to

claims 1, 12, 18, and 21 place these claims into condition for allowance over the 35 U.S.C. § 102(e) rejection based upon Takinosawa.

The present invention is directed to a built-in self-test circuit for testing a serializer/deserializer circuit. As defined in these claims, the serializer/deserializer circuit is a data processing circuit arranged to serialize and deserialize received parallel data into processed parallel data. More specifically, the built-in self-test (BIST) circuit comprises a transmit register that transmits parallel data to the data processing circuit, a receive register that receives the processed parallel data from the data processing circuit, and an error circuit that detects errors in the processed parallel data. Each of claims 1, 12, and 18 further define the error detector being coupled to the transmit register for receiving the transmitted parallel data from the transmit register and to the receive register for receiving the processed parallel data. It is respectfully submitted that Takinosawa fails to show or describe such structure.

Takinosawa is directed to a self test circuit for evaluating a high-speed serial interface. While it does disclose a BIST circuit and a BIST comparator for detecting errors, it does not show the BIST comparator being coupled to the BIST circuit for receiving the transmitted parallel data as defined in claims 1, 12, and 18. As a result, claims 1, 12, and 18 are respectfully considered not anticipated by Takinosawa and hence are considered to be in condition for allowance thereover. For the same reason, the rejected dependent claims 2, 5-7, 11, 14, 15, and 18 are considerable allowable over Takinosawa for the same reasons. Favorable reconsideration of these claims is also respectfully requested.

With respect to claim 21, claim 21 has been amended to recite that the testing step includes comparing the transmitted data to the processed parallel data. Again, this is not shown or described in Takinosawa. Favorable reconsideration of claim 21 and claim 22 which depends therefrom, is respectfully requested.

Claims 3, 4, 13, and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Takinosawa, in view of Fan et al., U.S. Patent Application Publication No. 2004/0030968. Claims 3 and 4 depend from claim 1, claim 13 depends from claim 12, and claim 23 depends from claim 21. Since each of these independent claims is considered allowable over Takinosawa as previous explained,

they are likewise considered allowable over the 35 U.S.C. § 103(a) rejection based upon Takinosawa and Fan et al. Further, while Fan does disclose the varying data length of data sequences to obtain error counting at high data rates, it is respectfully submitted that it does not amount to an expression of motivation for using data sequences of varying data length in a BIST circuit. Accordingly, it is respectfully submitted that claims 3, 4, 13, and 23 are allowable over the 35 U.S.C. § 103(a) rejection based upon Takinosawa and Fan et al.

Lastly, claims 8, 9, 16, 17, 20, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Takinosawa in view of Chen et al., U.S. Patent No. 5,726,991. In view of the amendments made to claims 1, 12, and 18, and the deficiencies in Takinosawa with respect to these claims, it is respectfully submitted that claims 8, 9, 16, 17, and 20 are clearly allowable over the combination of Takinosawa and Chen. Favorable reconsideration is respectfully requested.

With this amendment, the application is considered to be in condition for allowance. Such action is respectfully solicited.

DATED this 11th day of May, 2006.

Respectfully submitted,

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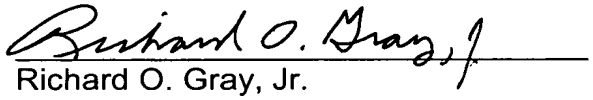

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